[0008] During the IC design, CAD tools are used that deal with timing constraints present throughout the circuitry. These tools provide timing analysis of circuit net lists and layouts by working in conjunction with the logic synthesis and physical design tools. EinsTimer is such a tool that is commercially available to provide this static timing analysis, made by International Business Machines Corporation, Armonk, NY, USA. Aspects of this tool are discussed in IBM Technical Disclosure Bulletin, Vol. 37, No. 9, pages 433-34 (September 1994) incorporated herein by reference. Presently used clock gating tests that are performed are between an arrival time (AT) at the gate output rather than at the gate input (i.e., between AT_{clock} + $delay_{clock}$ and AT_{gate} + $delay_{gate}$). In Figures 6A and 6B the signal arrival times and slew are represented as follows: AT_{clock} (ATc in the drawings), AT_{gate} (ATg in the drawings), $Slew_{clock}$ (Slew_c in the drawings), and $Slew_{gate}$ (Slew_g in the drawings).

[0051] The setup times determined by the second embodiment are compared against results of a simulation approach in FIG. 11. Then the projected setup time (from the above equations, using K = 0.5) was calculated and [subtracted from] the measured ("real") setup time determined through simulation to determine the error in the computed setup time was then subtracted from the projected setup time. A positive error is pessimistic (i.e., requires the disabling gate transition to arrive earlier than necessary), and a negative error is optimistic (i.e., allowing the disabling clock gate transition to arrive later than necessary). This is done over a very wide set of transistor widths, output capacitance loadings, and input slews (# of occurrances). The resultant error over various combinations of these parameters is shown in the histogram in FIG. 11, wherein the second embodiment of invention (modified propagated) is used and provides a tighter distribution than the original propagated method.